METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
BY FORMING DAMASCENE INTERCONNECTIONS

ABSTRACT OF THE DISCLOSURE

A method for fabricating a semiconductor device, in which a sufficient misalignment margin is obtained when forming interconnections and contact holes, is provided. Dielectric layer patterns which define recesses in which damascene interconnections are to be formed, are formed. Then, first contact holes between the dielectric layer patterns are etched, and the first contact holes and the recesses are concurrently filled with a conductive material. The recesses can be filled with the conductive material by performing an etch-back process. The dielectric layer patterns are then etched, thereby forming the damascene interconnections and concurrently covering only a region in which second contact holes are to be formed with the dielectric layer patterns. Spaces between the dielectric layer patterns are filled with a mask layer, and then the dielectric layer patterns are selectively removed from the resultant structure, thereby forming the second contact holes aligned with the damascene interconnections.